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REMARKS

Applicant appreciates the Examiner's thorough examination of the subject application and requests reconsideration of the subject application based on the the following remarks.

Claims 1-21 are pending in the subject application.

Claims 9-13, 19, 21, 23 and 26 are acknowledged as being allowable by the Examiner.

Claims 1 and 20 stand rejected under 35 U.S.C. §103. Claims 2-8, 14-18, 22, 24 and 25 were objected to as depending from a rejected base claim, however, the Examiner indicated that the claims would be allowable if appropriately re-written in independent form.

Claims 27 and 28 were added to more specifically indicate that the serial-to-parallel converter means/conversion circuit outputs the plurality of kinds of pulse signals at the time intervals represented by the single signal of serial data. The amendments to the claims are supported by the originally filed disclosure.

35 U.S.C. §103 REJECTIONS

Claims 1 and 20 stand rejected under 35 U.S.C. §103 as being unpatentable over Riggio, Jr. [USP 5,557,272; "Riggio"] for the reasons provided on pages 2-3 of the above-referenced Office Action. Applicant respectfully traverses as discussed below.

As grounds for the rejection the above-referenced Office Action asserts that Riggio teaches a data processing system including a non-volatile serial to parallel converter 34. It also is asserted that the non-volatile serial to parallel converter 34 receives through port 36, serial data supplied as DATA-IN signals on input line 38 and produces parallel output through the parallel data-output 40 port to the bus 42. It is admitted that Riggio does not teach a signal production circuit for producing pulse signals; however, the Office Action further asserts that it would have been obvious to one skilled in the art to replace the data processing system with an equivalent circuit since the preamble is generally not accorded any weight.

In this regard, Applicant would note that while there is extensive characterizing of Riggio in some detail in the Office Action, there is no clear indication in the Office Action as to what elements of Riggio allegedly correspond to the elements or features set forth in the claims of the subject application. Notwithstanding this, Applicant offers the following remarks and observations regarding the device, circuitry and operation described in Riggio.

As set forth in claim 1, Applicant claims a signal production circuit for producing a plurality of kinds of pulse signals, which are respectively repetitions of a predetermined sequence of pulses. Such a signal production circuit includes, *storage means* for storing, as digital data, a single signal of serial data including a time series of data pulses representative of all rise and fall timings of the plurality of kinds of pulse signals and data pulses representative of all time intervals between the rise and fall timings; and *serial-to-parallel converter means* for reading the signal of serial data from the storage means and producing, as parallel data, the plurality of kinds of pulse signals from the data representative of all the predetermined rise and fall timings of the plurality of kinds of pulse signals. It necessarily follows from the foregoing that the storage means is operably coupled to the serial-to-parallel converter means such that the signal of serial data stored in the storage means can be read by the serial-to-parallel converter means such that the signal of serial data is converted within the converter means so as to produce the plurality of parallel signals therefrom.

Applicants would first note that Riggio does not teach "serial data including a time series of data pulses representative of rise and fall timings of the plurality of kinds of pulse signals and data pulses representative of all time intervals between the rise and fall timings" and "producing, as parallel data, the plurality of kinds of pulse signals from the data representative of all the predetermined rise and fall timings of the plurality of kinds of pulse signals," as is set forth in claim 1. There simply is no teaching or suggestion in Riggio that the DATA IN signal (or any other signal described therein) is representative of rise and fall timings of the plurality of kinds of pulse signals, as claimed by Applicant. However, even if one were to assume that the DATA IN signal of Riggio was in some way representative of rise and fall timings (which Applicant does

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not admit is disclosed or taught in Riggio), the NON-VOLATILE SERIAL-TO-PARALLEL CONVERTER of Riggio does not produce as parallel data, a plurality of kinds of pulse signals that have timings represented by DATA IN. The NON-VOLATILE SERIAL-TO-PARALLEL CONVERTER of Riggio merely outputs the serial data as parallel data.

While Riggio does show a serial to parallel converter this is not the serial-to-parallel converter *means* as claimed by Applicant. A conventional serial to parallel converter is a device that converts sequential input from a serial transmission device and passes it on via the required number of parallel lines. In other words, the data is rearranged by a conventional serial to parallel converter. The teachings of Riggio, however, are not even a typical serial-to parallel conversion. The reference merely teaches that data coming in via DATA-IN is successively delayed or inverted. Riggio provides that in the normal mode of operation, "n" serial bits is written into the converter and then, following generation of a READ-OUT signal, "n" parallel bits are read out of the converter (see Riggio, col. 7, ll. 49-54).

The serial-to-parallel converter means of the present invention reads serial data contained in the storage means, and generates parallel pulse signals of different kinds based on the rise and fall timings of the serial data. That is, the function of the serial-to-parallel converter means of the present invention is not merely to rearrange data but to generate pulse signals based on the rise and fall timings of serial data. Thus, in this respect, the serial-to-parallel converter means of the present invention is clearly different, both structurally and functionally, from the serial to parallel converter disclosed and taught in Riggio.

An advantageous effect of the present invention is that effective use of data is made possible, through a special serial-to parallel conversion. For example, by simply entering a data signal into the CLOCK of a flip-flop (a regular CLOCK signal is not needed by the flip-flop), a single set of serial data is converted into data corresponding to all the parallel signals. Therefore, it is possible to read out a large number of signals timings (enormous amount of kinds of signals, depending on the circuit).

In contrast, the converting method of Riggio is as follows. The data signals are put in DATA of flip-flop, and output is conducted by taking in the data by using clock signals (CLOCK-A, CLOCK-B) separately prepared. This method however only causes the delay or the inversion of the original data. As such, for parallel data sets, it is not possible to set an independent logic for a single data set, or it is not possible to change the timing of a single data set.

That is and as was pointed above, Riggio does not describe anywhere timings of risings and fallings of a plurality of kinds of parallel data. Moreover, with the device of Riggio, it is not actually possible to independently modify the timing of the parallel data sets. Please see the attached diagram.

Furthermore, the circuitry/device of Riggio requires as the original signal three kinds of signals: *i.e.*, a data signal, CLOCK-A, and CLOCK-B, whereas the original signal is only a data signal in the present invention. Accordingly, the present invention is more advantageous than the device of Riggio, and yields unpredictably remarkable effects.

In this regard, Applicant also would direct the Examiner's attention to the attached sheet that illustrates examples of serial-to-parallel conversion according to the circuitry in Riggio and serial-to-parallel conversion that results from the signal production circuit of claim 1.

Riggio also describes the non-volatile storing of the data that is written to the converter so that if power is lost, the data stored in the converter is not lost. However, this storage of data in Riggio does not correspond to a storage means of claim 1, in particular as the data being stored in Riggio is the data being converted into parallel form.

As indicated above, the storage means of the present invention is operably coupled to the serial-to-parallel converter means. While there is an input of serial data to the serial to parallel converter in Riggio; Riggio does not anywhere describe storage of digital data in serial form, which data is used to produce the plurality of kinds of pulse signals which are respectively

repetitions of a predetermined sequence of pulses, described anywhere in Riggio. Thus, Riggio does not anywhere describe, teach or suggest providing the storage means as set forth in claim 1.

In sum, it is clear from the foregoing remarks that Riggio does not disclose, teach or suggest the storage means for storing, as the digital data, a single signal of serial data including a time series of data pulses representative of all rise and fall timing of the plurality of kinds of pulse signals and data pulses representative of all time intervals between the rise and fall timing of claim 1. It also is clear that the serial-to parallel converter described in Riggo does not describe, teach or suggest the serial-to-parallel converter means for reading the signal of serial data from the storage means and producing, as parallel data, the plurality of kinds of pulse signals from the data representative of all the predetermined rise and fall timings of the plurality of kinds of pulse signals of claim 1. It also is clear, that the discussion in Riggio does not provide any teaching, suggestion or motivation for modifying the circuitry shown in Fig. 3 so as to yield elements that correspond to the storage means and serial-to-parallel converter means of claim 1.

Applicant also would submit that based on the foregoing comments regarding claim 1, it also can be seen that Riggio does not describe, teach or suggest (a) a memory for storing, as the digital data, a single signal of serial data including a time series of data pulses representative of all rise and fall timings of the plurality of kinds of pulse signals and data pulses representative of all time intervals between the rise and fall timings and/or (b) a serial-to-parallel conversion circuit for reading the signal of serial data from the memory and producing, as parallel data, the plurality of kinds of pulse signals from the data representative of all the predetermined rise and fall timings of the plurality of kinds of pulse signals as are set forth in claim 20. It also is clear, that the discussion in Riggio does not provide any teaching, suggestion or motivation for modifying the circuitry shown in Fig. 3 so as to yield elements that correspond to the memory and serial-to-parallel conversion circuit of claim 20.

As provided in MPEP 2143.01, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the

knowledge generally available to one of ordinary skill in the art. *In re Fine*, 837 F. 2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F. 2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). As provided above, Riggio does not include such teaching, suggestion or motivation.

Furthermore, and as provided in MPEP 2143.02, a prior art reference can be combined or modified to reject claims as obvious as long as there is a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 19866). Additionally, it also has been held that if the proposed modification or combination would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. Further, and as provided in MPEP-2143, the teaching or suggestion to make the claimed combination and the reasonable suggestion of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). As can be seen from the forgoing discussion regarding the disclosures of Riggio, there is no reasonable expectation of success provided in Riggio of a signal production circuit such as that provided in claims 1 or 20. Also, it is clear from the foregoing discussion that the modification suggested by the Examiner would change the principle of operation of the circuitry, would change the intended purpose of such circuitry and would destroy the described circuitry all of which is described in Riggio so as to yield the signal production circuit set forth in either of claims 1 or 20.

The Federal Circuit has indicated in connection with 35 U.S.C. §102 that in deciding the issue of anticipation, the trier of fact must identify the elements of the claims, determine their meaning in light of the specification and prosecution history, and identify *corresponding elements* disclosed in the allegedly anticipating reference (emphasis added, citations in support omitted). *Lindemann Maschinenfabrik GMBM v. American Hoist and Derrick Company et al.*, 730 F. 2d 1452, 221 USPQ 481,485 (Fed. Cir. 1984).

Notwithstanding that the instant rejection is under 35 U.S.C. §103, in the present case the Examiner has not identified the elements in Riggio that allegedly correspond, as that term is used above by the Federal Circuit, in any fashion to the storage means and the serial-to-parallel

converter means of claim 1 or the memory and serial-to parallel conversion circuit of claim 20, as well as the arrangement thereof, in its entire claimed form as set forth in claims 1 and 20 of the present invention. Furthermore, the Office Action remarks do not show that the discussed elements from Riggio correspond, as that term is used above by the Federal Circuit, in any fashion to the storage means and the serial-to-parallel converter means of claim 1 or the memory and serial-to parallel conversion circuit of claim 20, as well as the arrangement thereof, in its entire claimed form as set forth in claims 1 and 20 of the present invention.

As provided by the Federal circuit, a 35 U.S.C. §103 rejection based upon a modification of a reference that destroys the intent, purpose or function of the invention disclosed in a reference, is not proper and the prima facie case of obviousness cannot be properly made. In short there would be no technological motivation for engaging in the modification or change. To the contrary, there would be a disincentive. *In re Gordon*, 733 F. 2d 900, 221 USPQ 1125 (Fed. Cir. 1984). In the present case it is clear that if circuitry described in Riggio was modified in the manner suggested in the Office Action, it would destroy the intent, purpose or function of the circuitry as taught by Riggio.

As the USPTO Board of Patent Appeals and Interferences has held, "The mere fact that a worker in the art could rearrange the parts of the reference device to meet the terms of the claims on appeal is not by itself sufficient to support a finding of obviousness. The prior art must provide a motivation or reason for the worker in the art, without benefit of appellant 's specification, to make the necessary changes in the reference device." *Ex parte Chicago Rawhide Mfg. Co.*, 223 USPQ351, 353 (BD. Pat. App. & Inter. 1984). It is clear from the foregoing remarks that the suggested modification to the circuitry in Riggio would require a modification to the operation of the disclosed device and/or is more than an obvious matter of design choice.

It is respectfully submitted that for the foregoing reasons, claims 1 and 20 are patentable over the cited reference(s) and thus, satisfy the requirements of 35 U.S.C. §103. As such, these claims are allowable.

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CLAIMS 2-8, 14-18, 22, 24 & 25

In the above-referenced Office Action, claims 2-8, 14-18, 22, 24 and 25 were objected to as being dependent upon a rejected base claim. It also was provided in the above-referenced Office Action, however, that these claims would be allowable if rewritten in independent form to include all the limitations of the base claim and any intervening claim(s).

In as much as Applicant believes that the respective base claims (claims 1 and 20) are in allowable form, claims 2-8, 14-18, 22, 24 and 25 were not re-written in independent form as suggested by the Examiner. Applicant, however, reserves the right to later amend the subject application so as to present any one or more of these claims in independent form or to add one or more independent claims that contain the limitations of any one or more of claims 2-8, 14-18, 22, 24 and 25.

CLAIMS 27 and 28

As indicated above, claims 27 and 28 were added to more distinctly claim that the serial-to-parallel converter means/conversion circuit outputs the plurality of kinds of pulse signals at the time intervals represented by the single signal of serial data. These claims are clearly supported by the originally filed disclosure, including the originally filed claims.

It also is respectfully submitted that these added claims are patentable over the cited prior art on which the above-described rejection(s) are based. Under normal operation, the NON-VOLATILE SERIAL-TO-PARALLEL CONVERTER of Riggio outputs the parallel data of all cells to be read at the same time, when a READ-OUT signal is received (see Riggio column 7, lines 61-65). Thus Riggio can not teach or suggest the above feature.

It is respectfully submitted that the subject application is in a condition for allowance. Early and favorable action is requested.

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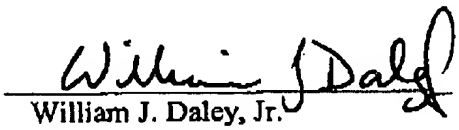
Because the total number of claims and/or the total number of independent claims post amendment now exceed the highest number previously paid for, authorization is provided herewith to charge the below-identified deposit account for the required additional fees. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, the Commissioner is hereby authorized and requested to charge Deposit Account No. **04-1105**.

Respectfully submitted,
Edwards Angell Palmer & Dodge, LLP

Date: November 9, 2006

By: 

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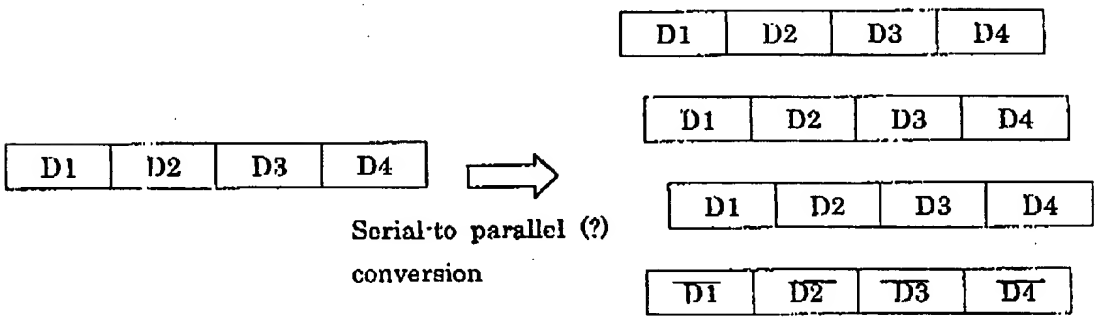
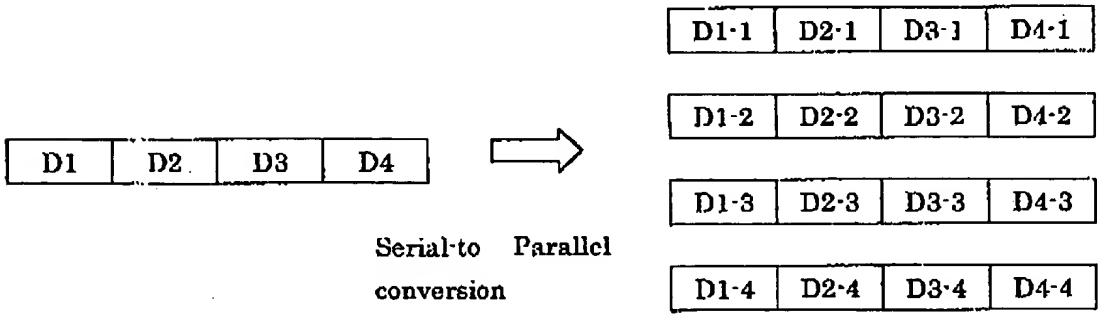
Attachment to Response

Example of serial-to parallel conversion result according to the device of Riggio.



4 data sets are no more than the original data which is delayed or

Example of serial-to parallel conversion result according to the present invention.



16 data sets are completely independent.